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Session 1224

The Third Porting: Applying Past Lessons to the Alpha/Itanium Transition

Friday, October 11, 2002
9:30 – 10:45
Room 122

This session is about –

- Technical review
- Issues in porting
- History and context of EPIC (CISC, RISC, EPIC)
- Technical emphasis
- Sizing and migration

This session is NOT about –

- Marketing
- Non-disclosure material
- Product sales strategies

In the interest of transparency –

- I have never been an employee of Digital/Compaq/HP/Intel
- I do have a small holding in HP stock
- I am not presently a consultant to HP/Intel
- None of the material is derived from a Non-Disclosure
- The opinions expressed are purely my own

Don’t know means DON’T KNOW –

- But we can make reasonable analyses based upon published data
  - Published Alpha specifications
  - Published Itanium(tm) specifications
  - OpenVMS documentation set
  - Digital Technical Journal

Don’t know means DON’T KNOW (cont’d) –

- and upon applicable experience
  - PDP-11 to VAX (1978 – present)
  - VAX to Alpha (1992 – present)
  - General experience

My personal background –

- 25 years of experience on multiple platforms
- Platforms (integer size/address size/integer format)
  - IBM System/360/370 (32/24/2)
  - Digital PDP-11 (16/16/2)
  - Digital VAX (32/32/2)
  - CDC 6600 (60/18?/1)
  - Digital PDP-10 (36/?/2)
  - Compaq Alpha (64/64/2)
  - Intel 808x (16-32/?/2)
  - Intel IA-32 (32/?/2)

My personal background (cont’d) –

- Compiler code generator developer
- uncompleted PhD research
- FPS-164 array processor experience
- Portable software developer

Architectural Attributes

	PDP-11	VAX	Alpha	Itanium
Architecture Type	1/2 Address	CISC	RISC	EPIC
Address Size	16	32	64	64
Integer Size	16	32	64	64
Byte Order	little	little	little	little
Alignment	word	none	quad	quad

Architectural Attributes – PDP-11 versus VAX

	PDP-11	VAX	Alpha	Itanium
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- same character set
- same integer style (two’s complement)
- different word size – 16 bit versus 32 bit
- different address size – 16 bit versus 32 bit
- different instruction set philosophy

Architectural Attributes – VAX versus Alpha

	PDP-11	VAX	Alpha	Itanium
Architecture Type	1/2 Address	CISC	RISC	EPIC
Address Size	16	32	64	64
Integer Size	16	32	64	64
Byte Order	little	little	little	little
Alignment	word	none	quad	quad

- same character set
- same integer style (two’s complement)
- different word size – 32 bit versus 64 bit
- different address size – 32 bit versus 32/64 bit
- different floating point formats
- different instruction set philosophy – CISC versus RISC

Architectural Attributes – Alpha versus Itanium

	PDP-11	VAX	Alpha	Itanium
Architecture Type	1/2 Address	CISC	RISC	EPIC
Address Size	16	32	64	64
Integer Size	16	32	64	64
Byte Order	little	little	little	little
Alignment	word	none	quad	quad

- same word size – 64 bit
- same address size – 64 bit
- same floating point formats
- same character set
- same integer style (two’s complement)
- different instruction set philosophy – RISC versus EPIC

Porting –

- Cross Platform/OS (Solaris C/C++ to OpenVMS Alpha)
- Cross O/S (OpenVMS C/C++ to Tru64 C/C++)
- Cross Platform/Same OS (OpenVMS VAX to/from Alpha)

Porting Difficulty –

	Operating System	
	Same	Different
Same Platform	0	10*
Different Platform	1	15*

* Highly Application Sensitive

- historically, porting has meant change in OS and architecture
- the data supports the conclusion that change in OS is the source of more problems
- OpenVMS, LINUX, DII COE, and other examples standardize interfaces (APIs) across multiple CPU architectures

Itanium Issues–

- Atomicity
- Precision
- Address Size
- Granularity
- Alignment
- Byte Ordering

Atomicity –

- on VAX, INCx was accidentally thread atomic
- on Alpha, translated as load/add/store
- Alpha translation was not safe
- accidental atomicity was not part of the spec
- solution – use ADAWI

Precision –

- VAX and ALPHA – different floating point and integer sizes/formats
- Alpha and Itanium – same precision/formats

Address Size –

- VAX – 32 bits
- Alpha/Itanium – 64 bits
- VAX to Alpha required data structure changes

Granularity –

- VAX was byte aligned for all operands
- VAX was prone to fractured loads/stores
- Alpha/Itanium require natural alignment

Data Alignment –

- VAX was byte aligned – all operands
- Alpha/Itanium require natural alignment
- No difference between Alpha/Itanium

Byte Ordering –

- VAX is little endian (low byte addressed)
- Alpha is little endian
- Itanium operates little/big endian

History and Context of EPIC –

- Alpha antecedents include IBM System 360/91
- Itanium descended from VLIW, and microcode
- Itanium is more dependent on compilers
- compiler dependency is not new
- EPIC presumes (correctly) that virtually all code is generated by compilers

Technical Emphasis –

- from a programming level Itanium and Alpha have similar restrictions
- there are few technical/programming impediments to porting applications between Alpha/Itanium

Sizing and Migration–

- sizing (speed and/or size) is quite application sensitive
- strategy – get smallest/cheapest system
- do science – DO NOT guess
- optimization may have substantial impact

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Session Notes & Materials:
http://www.rlgsc.com/hpets/2002/index.html

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Questions?